International Journal of Electronics Engineering (ISSN: 0973-7383)
Volume 10 • Issue 2 pp. 648-664 June 2018-Dec 2018 www.csjournals.com

# Modeling and Simulation of Hilbert Transform Phase Detector Based on All Digital PhaseLocked Loop

Alpana A. Deshmukh [1*], R. S. Gamad[2], D. K. Mishra[3]

[1]Research Scholar of E &T.C. Engineering department, Shri G. S. Institute of Technology and Science, Indore, Madhya Pradesh, India,deshmukhalpana81@gmail.com
[2] H.O.D of E & I Engineering department, Shri G. S. Institute of Technology and Science, Indore Madhya Pradesh, India,rsgamad@gmail.com
[3]Professor of E & I Engineering department, Shri G. S. Institute of Technology and Science, Indore Madhya Pradesh, India,mishradrc@gmail.com

**Abstract:**Phase Locked Loop (PLL) is one of the important components in various RF signal processing systems. In this area, various improvements over basic PLL scheme occur like digital PLL and All Digital PLL (ADPLL) etc. In recent area of research, ADPLL is used in modern electronic communication systems like frequency synthesizer, modulator, demodulator etc. In this paper, modeling & simulation work of Hilbert phase detection based on ADPLL is described. The Hilbert transform based phase detection system reports various advantages over conventional analog phase detector system. The noise performance locking improvement is reported in the paper for different steps of locking time. The noise response is reduced up to -145dBc/Hz in proposed work but previously it was up to -78dbc/Hz @ 20 kHz offset.The spectrogram of the PLL output signal for step change in reference frequency is described for locking time of PLL. The improvements are obtained in results as given in table 1.

**Keywords:**Phase Locked Loop, All Digital Phase Locked Loop, Voltage Controlled Oscillator, Digital Controlled Oscillator and Digital Phase Lock Loop etc.

## Introduction

### PLL

It is an important element in signal processing system. It is a feedback system which require external input signal & generates the phase locked signals. These are most common component for RF signal detection. These are used for generating the output signal whose frequency is programmable, rational multiple of a fixed input frequency. In other word, frequency and phase of the input signal is locked by PLL. When the phase and frequency of the input signals are synchronized, the PLL will consider under locked condition [1, 2]. The phase difference between the output signal and the reference is a known value when the loop is locked.A PLL is an electronic circuit with a VCO that constantly adjusts the phase of PLL output signal to match the frequency of an input signal. PLL is very much desired for faster and efficient operations in various areas of electronics [3].
Basic block diagram of PLL is shown in figure 1.

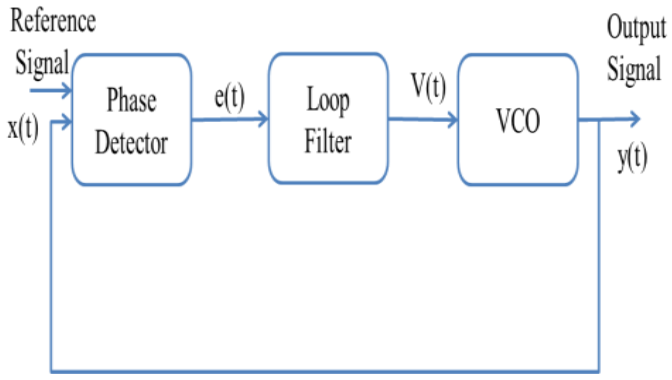


Figure1. Block diagram of Phase-Locked Loop

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**All Digital PLL**

ADPLL designs are portable for different applications with various ranges of frequency & to allow adoption for semiconductor technologies. ADPLL includes TDCs with noise shaping of the quantization error. With the advancement in mixed signals based circuits, research work is mostly focuses on ADPLL [3].

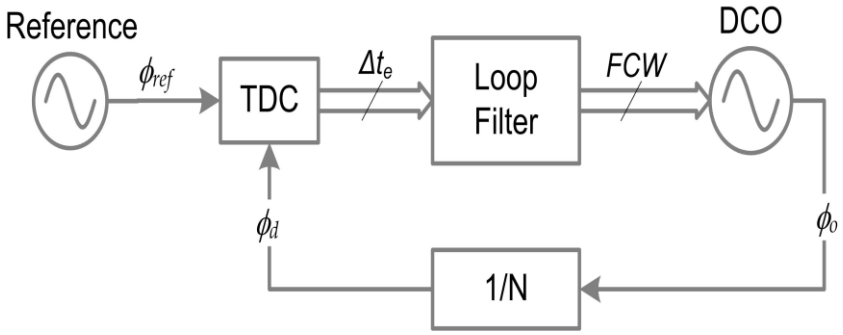


Figure 2. General block diagram of ADPLL

An ADPLL is characterized by the absence of analog signals other than the Local Oscillator (LO) Radio Frequency (RF) signal, the Reference signal, and the frequency divider output. While the analog nature of the LO RF signal is clear, the analog nature of the typically squared wave reference and the divider output signals may be in doubt. The analog nature of all these signals is inherent in their timing and thus in their phase. A block diagram of an ADPLL is shown in figure 2.

**TDC**

A time to digital converter is an electronic instrument to understand events & representing inputs in the form of time intervals. It is a device which is mostly used to measure time interval & convert it in to binary form, it also known as time counter. It shows the output between reference frequency and DCO output frequency. It is also useful in many time related applications in the field of electronics. TDC digitalizes the delay between the divider output and the reference signal replacing the analog phase detector as shown in figure 2. For better long term stability, it uses a crystal oscillator reference frequency. To get better reception a PLL frequency multiplier can be used to generate a faster clock [4] [5].

**Digital Loop filter**

It does not have passive components like resistor and capacitors. Here UP/DOWN counter is used as a loop filter which is useful for phase frequency detector. ADPLL having a conventional bang system in which locking time sturdily relies on the bandwidth of the system determines how much phase error a PLL can correct a cycle? For a first order system, the locking time can be determined as [6].

$$t_{lock} = \frac{\Pi}{\left[ 2\Pi / f_{ref} * \left( \beta k_{vco} - f_{off} \right) \right]} \quad (1)$$

$f_{ref}$is the reference clock frequency,β is the proportional gain, and$f_{off}$ is the initial frequency error.

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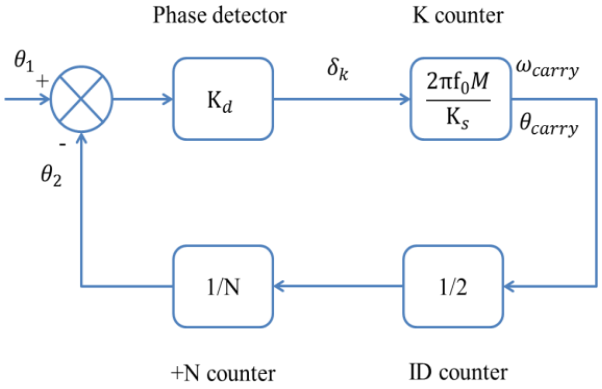


Figure 3. Frequency Domain Analysis of the ADPLL

Figure 3 has represented the frequency domain analysis of the ADPLL.

$K_d=2/\pi$ (2)
$K_d$ = Phase detector output
Model for the K- counter [4]:

$$f_{carry} = \delta_k \frac{M f_o}{k} \rightarrow \omega_{carry} = 2\pi\delta_k \frac{M f_o}{k} \quad (3)$$

Transfer function of the K-counter [4]:

$$k_k(s) = \frac{\theta_{carry(s)}}{\Delta_{k(s)}} = \frac{1}{s}\frac{\omega_{carry}}{\delta_k}\frac{2\Pi\delta_k}{sk} \quad (4) \qquad \theta_2(s) = \frac{1}{N}.\frac{1}{2}\frac{2\Pi M f_0}{sk} k_d \left[\theta_1(s) - \theta_2(s)\right] = \frac{k_d \Pi M f_0}{sNk}\left[\theta_1(s) - \theta_2(s)\right] \quad (5)$$

$$\theta_2(s) = \frac{\omega_0}{s}\left[\theta_1(s) - \theta_2(s)\right] \rightarrow \frac{\theta_{2(s)}}{\theta_{2(s)}} H(s) = \frac{\omega_0}{s+\omega_0} \quad (6)$$

$$\omega_0 = \frac{K_d \Pi M f_0}{NK} or \tau = \frac{1}{\omega_0}\frac{NK}{K_d \Pi M f_0} \quad (7)$$

Where,

M, N, K are counter in mostly powers of 2, $k_k$ = Transfer Function, $\omega_{carry}$ =Angular frequency for Carrier signal,

$f_o$ =Output frequency,

$\theta_1(s), \theta_1(s)$ = Phase angle, $\delta_k$ = Duty factor,

$\omega_0$ = Output angular frequency, $f_0$ = Output frequency, Here

$$\tau = \frac{NK}{2\Pi M f_0} \quad (8)$$

**DCO**

Digitally Controlled oscillators are nothing but a customized oscillator The DCO gets the signals from LF and makes closer to the input signal. It is designed using the digital devices. The time domain analysis is better than the voltage domain analysis. It is operated with digital inputs and digital outputs in the discrete time domain, although it is a continuous time and in general continuous amplitude. To realize an ADPLL, existing elements must be digital circuits. The DCO comes under the digital model of the VCO in DPLL. The +N counter is used for high frequency oscillations ($f_{ref}$). The Digital Loop filter controls the +N bit output operation of the DCO. eq. (9) represents the output frequency of DCO [6]. Here in fig 3 a simple ÷N counter works as DCO. High frequency signal operates at very high frequency. Divide by N counter produces N bit parallel output. Jitter can't design with the help of this type of DCO.

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$$f_{Dco} = \frac{f_{ref}}{Nf_{DCO}} = \frac{f_{ref}}{N} \quad (9)$$

Ring oscillators are widely used here for generating multi-phase clock outputs. The minimum number of stages required to produce oscillation in ring oscillators are three.

**ADPLL Functional Model and Discussion**

PLLs are used in the digital domain, this means phase frequency detector, loop filter and VCO need to be converted to discrete-time system. Using an appropriate transformation, the loop filter can be converted from Laplace to the z-domain (e.g. Zero-Order Hold, Bilinear etc) [5, 6]. The top level module of the design is simulated in Simulink and implemented module is shown in the fig. 6. Here phase detector, produces the Up Down pulses which are fed as inputs to the increment decrement counter followed by DCO to control the voltage and align the frequency.

The Functional Model of ADPLL is shown in the figure 4.

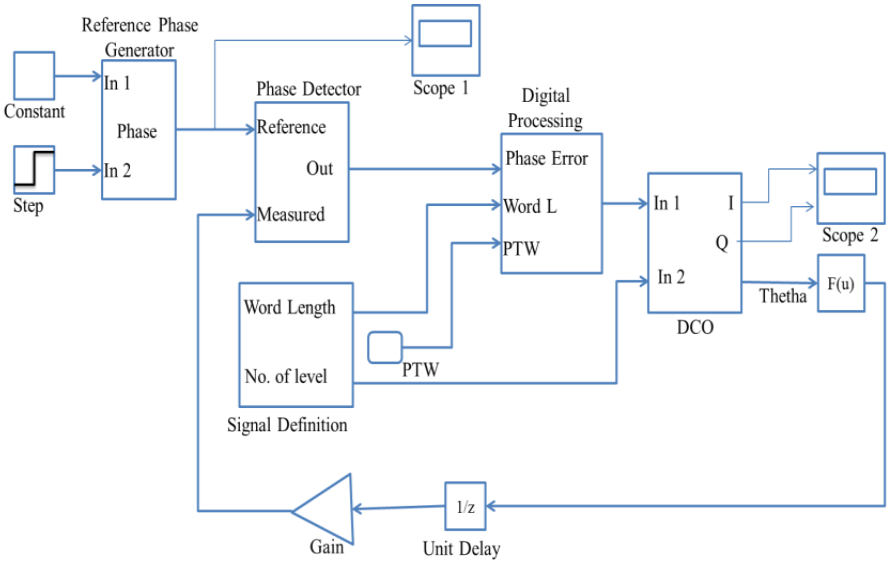


Figure 4. Functional model of ADPLL

IIR filter are used for loop filter. The general equation of filter is shown in equation (11) [12]

$$\frac{y_n}{x_n} = \frac{a_0 + a_1 z^{-1} + \text{-------} a_n z^{-n}}{b_{0|} + b_1 z^{-1} + \text{--------} b_n z^{-n}} \quad (10)$$

$$H(Z) = \frac{0.0148z - 0.0147}{z^2 - 1.985z + 0.9853} \quad (11)$$

Where $y_n$ = Output Sequence of IIR filter, $x_n$ = Input Sequence of IIR filter.The H (z) is the transfer function in Z-domain.

Hilbert phase detector, loop the different subsystem like DCO, phase detector, digital filters etc are modeled and connected to make the complete model of ADPLL. Word length of 32 bits has been chosen to have good resolution of phase detection. Filter and DCO are key development for ADPLL simulation.[7,8]. The Hilbert phase detector is shown in the figure 5. The phase detector response has been analysed seperatly. The input signal for phase detctor is given as $Sig_1(t) = Cos(\omega ot+\theta e)$ and the DCO output of the signal is given as $Sig_2(t) = Cos(\omega ot)$.

Where , $Sig_1(t)$ = Reference Frequency

$Sig_2(t)$ = Measured Frequency.

Then the phase error is given in eq.(12).

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$$\theta_e = \left[ \frac{\cos\omega_0 t \cos(\omega_0 t + \theta_e) + \sin\omega_0 t \sin(\omega_0 t + \theta_e)}{\cos\omega_0 t \sin(\omega_0 t + \theta_e) + \sin\omega_0 t \cos(\omega_0 t + \theta_e)} \right] \quad (12)$$

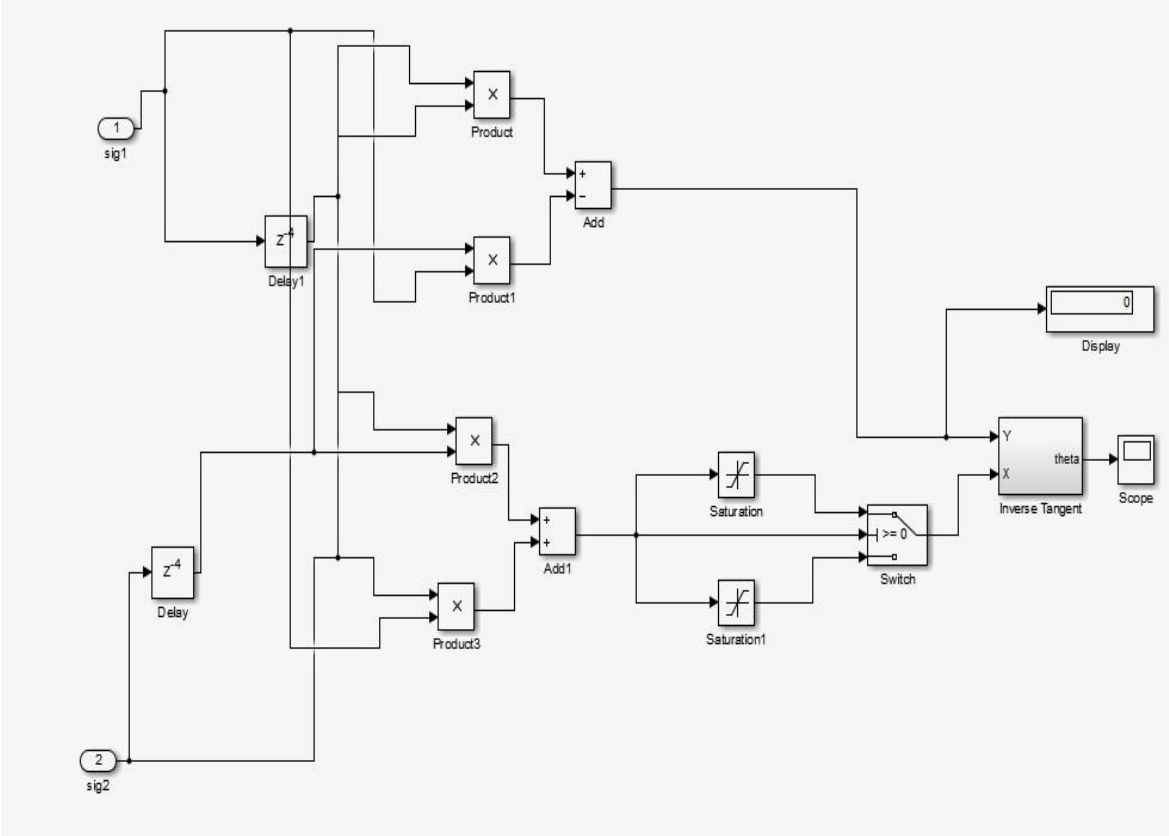


Figure 5. Functional model of Hilbert Phase Detector

**Results and Discussions**

The ADPLL model is simulated to identify the lock in time. Loop locked with input signal within 100 ns from reference output frequency is shown in figure 6. Whenever reference frequency will vary, the output response of ADPLL will also change with a slope of frequency change and stable after the locking time. The ADPLL response is observed with respect to changes in frequency of input signal, amplitude of PLL output will also change. Figure 7 represents frequencies in the output and multiple side-bands due to finite period of one of reference frequency. To have clearer picture, PLL spectrogram output is shown in figure 8. The figure 8 and figure 9 report the PLL response for change in frequencies.The lock-in time of ADPLL is 100 ns which are improved than earlier reported work [12]. Figure 9 also shows the transient time analysis of the PLL. Yellow colour represents high amplitude of the PLL and blue colour represents lowamplitude of the PLL. PLL response can be differentiating easily with the help of spectrogram of the system.

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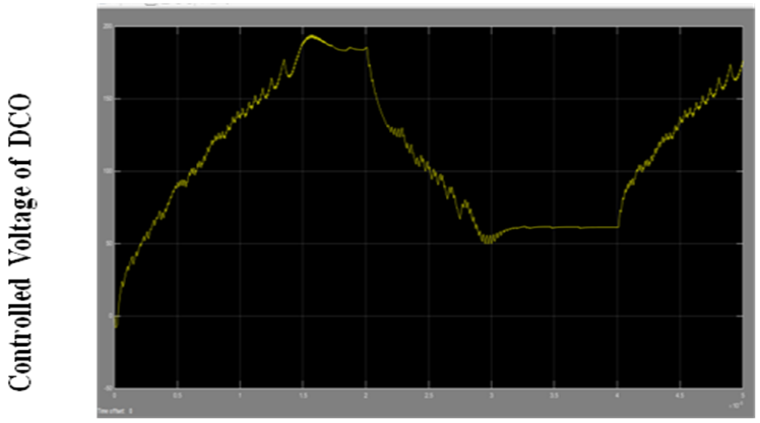


**Change in frequency at t=100 nanosecond**

Figure 6. DCO output of locking process

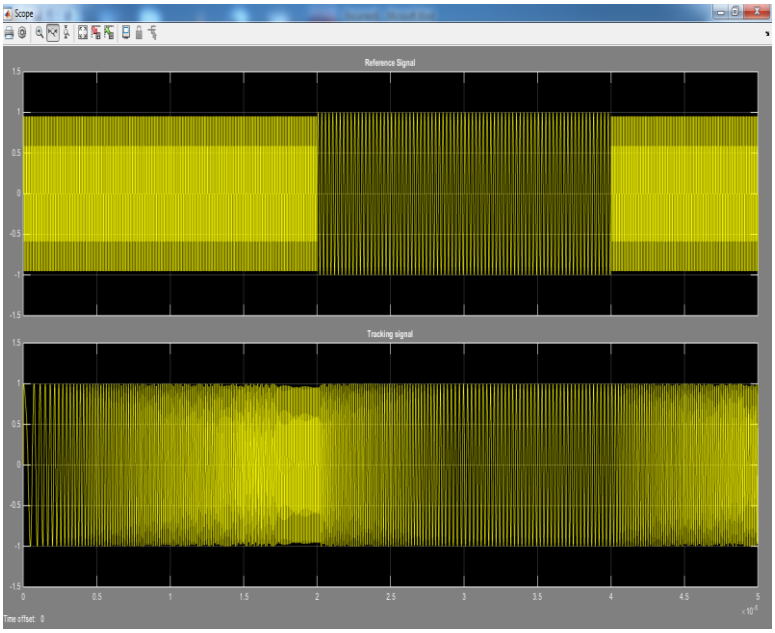


Figure 7. PLL output for reference frequency change

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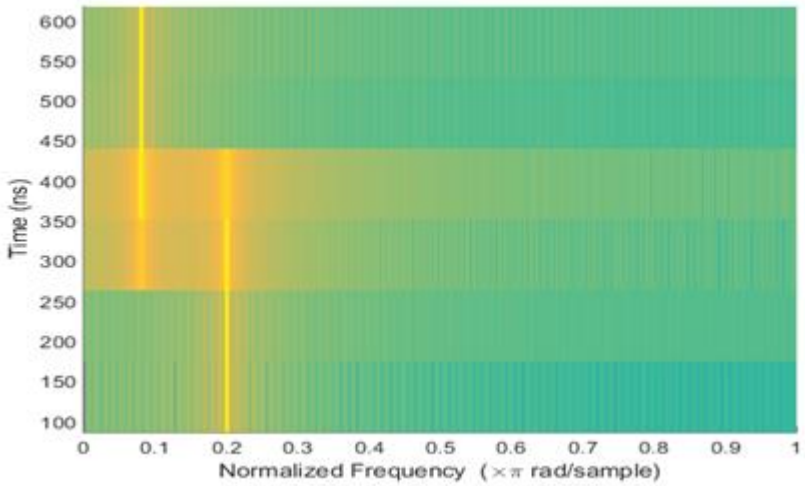


Figure8. Spectrogram of DCO output for variation in frequency of input signal

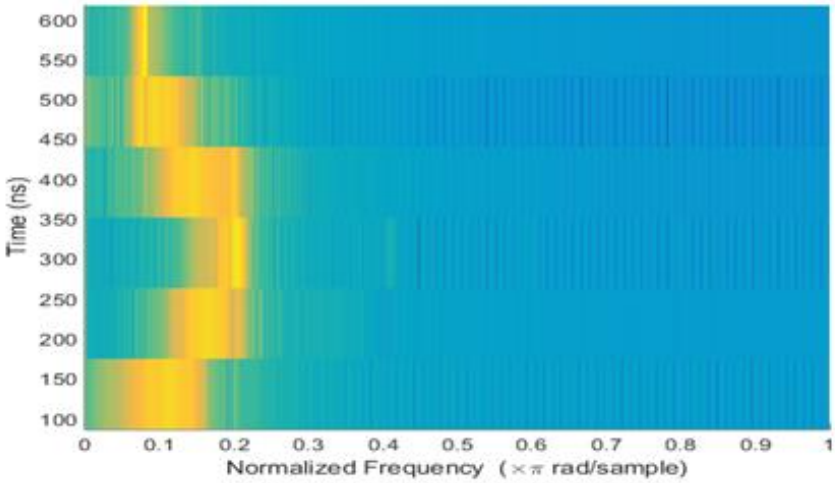


Figure 9. Spectrogram of DCO output for variation in frequency of input signal

Table 1 Comparison of various parameters in noise signal spectrum

| Parameter | Previous Work [12] | Proposed work |
|---|---|---|
| Reference Frequency | 26 MHz | 33 MHz |
| VCO free running frequency | 1339 MHz | 1339 MHz |
| VCO Sensitivity | 155.5 MHz/V | 300 MHz/V |
| Output Frequency Range | 1365 – 1676 MHz | 1300 -1700 MHz |
| Noise | –78 dBc/Hz @ 20 kHz offset | –145 dBc/Hz@20khz offset |

## Conclusion

Modeling and simulation of an ADPLL has been described in this paper. The Hilbert phase detector is used in the model of ADPLL for noise reduction in the output. The results are compared with the earlier reported work and improvements are obtained in noise performance and sensitivity due to the digital nature of the 32 bit ADPLL design. Author have also observed and achieved fast locking time (in nano second) during the simulation with same input signal.

## Acknowledgment

Simulation work has been done in research center SGSITS Indore. The authors would like to thank research center & its staff members for helpful discussions.

## Author's Profile

Author received B.E. degree in E & TC Engineering from SGSITS, Indore Madhya Pradesh and M.E. in Digital Instrumentation from DAVV (IET) Indore Madhya Pradesh in 2007.

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